Dual Degree Project Report

on

Simulation and Characterization of SOI MOSFETs

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by

Aatish Kumar
Roll No. 96D07039

under the guidance of

Prof. V. Ramgopal Rao

and

Prof. Rakesh Lal

Department of Electrical Engineering
Indian Institute of Technology
Mumbai
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Chairman : ________________  External Examiner : ________________

Guide : ________________  Internal Examiner : ________________

Co-Guide : ________________
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Aatish Kumar
(96D07039)

IIT Bombay,
Abstract

One of the most important parameters for the evaluation of fabrication quality and reliability of MOS devices is the interface state density. However, most of the techniques developed for bulk silicon technology are not applicable in Silicon-on-Insulator (SOI) devices owing to the absence of body contact as well as the complex multi-interfacial nature of these devices. A multi frequency transconductance technique has been developed and used to study the evolution of density of interface states with hot carrier stress in JVD SOI MNSFETs. The technique has been validated by charge pumping measurements on bulk MOSFETs.

Minimization of off-state leakage currents is an important issue in high-density, very low power, battery powered CMOS technologies. The off-state Gate-Induced-Drain-Leakage (GIDL) current, caused by band-to-band tunneling in the gate-drain overlap region, therefore, assumes greater significance. Gate Induced Drain Leakage (GIDL) current studies on conventional and lateral asymmetric channel (LAC) SOI MOSFETs have been carried out to extract the current gain of the parasitic bipolar transistor inherently present in these devices. It has been shown that the LAC structure leads to alleviation of floating body effects by suppressing the current gain of parasitic bipolar transistor.
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Chapter 1

Introduction

The idea of realizing semiconductor devices in a thin silicon film, which is mechanically supported by an insulating substrate, has been around for several decades. The first description of the insulated-gate-field-effect-transistor (IGFET), which later on evolved into the modern silicon metal-oxide-semiconductor field-effect-transistor (MOSFET), is found in the historical patent of Lilienfield dating from 1926. This patent depicts a three-terminal device where what is nowadays called a source-to-drain current is controlled by field effect from a gate which is dielectrically insulated from the rest of the device. The piece of semiconductor, which constitutes the active part of the device, is a thin semiconductor film deposited on an insulator. In a sense, it can thus be said that the first MOSFET was a Semiconductor-on-Insulator (SOI) device. The technology of that time was unfortunately unable to produce a successfully operating Lilienfield device. IGFET technology was then forgotten for a while, completely overshadowed by the enormous success of the bipolar transistor, discovered in 1947 [1]. It was only years later, in 1960, that Kahng and Atalla realized the first working MOSFET [2], when technology had reached a level of advancement sufficient for the fabrication of good quality gate oxides.

1.1 Motivation

Modern MOSFETs made in bulk silicon are far from the ideal structure described by Lilienfield. In a MOSFET, only the very top region (0.1-0.2 µm thick) of the silicon wafer is actually useful for electron transport. The inactive volume, more than 99.9 % of the wafer, induces only undesirable, parasitic effects. Interaction between the devices and the substrate gives rise to a range of parasitic effects, like the parasitic capacitance between diffused sources and drain and substrate, and latchup which consists of unwanted triggering of a PNPN thyristor structure inherently present in all bulk CMOS structures.
SOI devices emerged from the idea of separating or isolating the active device overlay from the detrimental influence of the underlying silicon substrate. Using SOI substrate, quasi-ideal devices can be fabricated. The full dielectric isolation of the devices prevents the occurrence of most of the parasitic effects experienced in bulk devices.

SOI has a number of advantages over bulk technology. Studies [3] show increased drain currents, and quasi-ideal subthreshold slopes, besides those listed above. The reduction of parasitic capacitances and increment in drain current increases the speed of the device. However, deep sub micron SOI MOSFETs suffer from short channel effects and these can be alleviated using appropriate channel engineering. One such structure called Lateral Asymmetric Channel (LAC) device [4,5] has been shown to have higher drain currents and better resistance to hot carrier resistance than conventional uniform channel devices. Therefore, the comprehensive study of LAC devices in order to study its performance vis-à-vis that of uniform channel device gains paramount importance.

Interface state characterization in small geometry MOSFETs with novel gate dielectrics is a subject of intensive research. However, most of the techniques developed for bulk silicon technology [6-9] are not directly applicable for SOI devices due to a number of reasons, the most prominent being the lack of substrate contact in addition to the complex multi-interface nature of these devices. Silicon nitride is being considered as a promising candidate to replace thermal oxide gate dielectric, as the latter is reaching its scaling limit due to the excessive increase in gate tunneling leakage current. Recently, Jet-Vapor-Deposited (JVD) nitrides have been shown to have excellent electrical properties as a gate material in terms of lower gate leakage, competitive transconductance, drain current drive and interface quality, compared to thermal SiO₂ [10]. Detailed electrical characterization of sub-100 nm bulk MNSFETs has also been reported with JVD SiN as gate dielectric [11]. Since silicon nitride has lower energy barrier for both holes and electrons, it is very essential to study its hot-carrier reliability in order to establish it as a viable alternative for silicon oxide as gate dielectric.

Next, a brief overview of the report is presented which describes the organization of various chapters and discusses the contents of each chapter in brief.
1.2 Chapter Overview

Chapter 2 discusses briefly about SOI materials and describes the working of an SOI transistor.

Chapter 3 attempts to compare SOI and bulk technologies in order to bring out the advantages and disadvantages of SOI technology vis-à-vis bulk technology.

Chapter 4 describes the basic characterization results obtained on thin film conventional and Lateral Asymmetric Channel (LAC) SOI MOSFETs and discusses some simulation results obtained using process simulator, TSUPREM-4 and device simulator, Medici.

Chapter 5 details gate induced drain leakage (GIDL) current studies performed on SOI MOSFETs and discusses its use in extraction of parasitic bipolar transistor current gain $\beta$ in these devices.

Chapter 6 discusses the multi-frequency transconductance technique, which has been proposed and implemented to extract interface state density in SOI MOSFETs and its application in studying hot-carrier performance of Jet Vapor Deposited (JVD) SOI MNSFETs.

Chapter 7 summarizes the work done and discusses the future scope of this work.
Chapter 2

A Brief Introduction to SOI Technology and Device operation

2.1 SOI Technology

SOI technologies can be in general divided into two groups. In the first, a thin insulating layer is used to separate the active semiconductor layer from the semiconductor substrate. These include Separation by IMplantation Of OXygen (SIMOX), Zone Melting Recrystallization (ZMR), Full Isolation by Porous Oxidized Silicon (FIPOS), and Wafer Bonding (WB). In the second group, the semiconductor film is deposited directly onto an insulating substrate. This is the case for Silicon On Sapphire (SOS) and Silicon On Zirconia (SOZ).

2.1.1 Separation by Implantation of Oxygen (SIMOX)

SIMOX [12] is considered to be the most advanced and promising of SOI technologies for high density CMOS circuits. The buried oxide is synthesized by internal oxidation during the deep implantation of oxygen ions into silicon. A postimplantation annealing is necessary to recover the crystalline quality of the Si overlay. High current implanters (150-200 mA) have been specially designed to produce large-diameter SIMOX wafers with excellent purity and homogeneity. Following are the milestones in the development of SIMOX structures.

1. Shallow implantation of oxygen into Si wafers leads to oxygen precipitation.
2. High-dose implantation (\(-10^{18} \text{ O}^+ \text{ cm}^{-2}\)) forms a stoechiometric SiO\(_2\) layer at the wafer surface, which demonstrates the feasibility of SIMOX.
3. Deep Implantation at high energy (>= 150 keV) allows the synthesis of a buried oxide 0.2-0.4 \( \mu \text{m} \) thick underneath a thin Si film.

4. Annealing at low temperature (LTA: 1150-1200 \( ^\circ \text{C} \)) results in an inhomogeneous Si film in which only the upper 0.1 \( \mu \text{m} \) thick region stands as a good quality crystal. The bottom interfacial region is still greatly disordered and contains many defects.

5. High-temperature annealing (HTA: 1250-1405 \( ^\circ \text{C} \)) improves and simplifies the vertical SOI structure. The high quality device-grade region extends over the whole film, and the interfaces become sharp.

In regular quality SIMOX wafers, the buried-oxide interfaces are sharp and uniform. The density of traps and fixed charges at the upper interface of the buried oxide is typically in the range of \( D_{it2} \sim 0.5-2 \times 10^{11} \text{ cm}^2 \text{eV}^{-1} \). It is definitely larger than that at the interface between film and gate oxide \( D_{it1} \sim 10^{10} \text{ cm}^2 \text{eV}^{-1} \), as in bulk Si), but, small enough not to adversely affect the performance of integrated circuits. In conclusion, although the SIMOX synthesis may appear to be a seemingly destructive process, it does result in device-grade SOI structures. The thin silicon layer is wafer-scale monocrystal with high quality and excellent electrical properties. The interface sharpness, the homogeneity, and the overall flexibility of engineering the structure represent sound arguments that promote SIMOX as the most suitable technology for thin-film applications.

**Fig. 2.1:** Fabrication of SIMOX Wafers
2.1.2  Zone Melting Recrystallization (ZMR)

ZMR [13] technology produces SOI structures by recrystallization of polysilicon films, deposited on oxidized silicon wafers. In the ZMR process, a thermal oxide (1-2 µm thick) is first grown on a bulk silicon substrate, followed by deposition of LPCVD amorphous or polycrystalline silicon film (0.5-1.0 µm thick) on the thermal oxide. The whole structure is capped with a 2 µm thick layer of deposited thermal oxide covered by a thin Si$_3$N$_4$ layer. A melting zone is scanned across the entire silicon wafer. As a result, full liquid phase recrystallization of silicon wafer can be carried out in a single pass.

The predominant defects that hamper the wide application of ZMR SOI materials are grain subboundaries. These are usually parallel to the scanning direction. The misorientation of the subboundaries is near 1° and the resulting stress causes the formation of dislocation arrays.

2.1.3  Full Isolation by Porous Oxidation Of Silicon (FIPOS)

FIPOS [14] involves the use of oxidized porous silicon. This technique is more complicated than the SIMOX and ZMR processes, but offers the potential for essentially defect-free active silicon layers. The process is relatively clean. Oxidation of the porous silicon layer leads to the standard thermal oxide and does not disturb the high quality of the original silicon film.

The key aspect in FIPOS technique is the formation of porous silicon, which is controlled by the type and concentration of doping as well as by the current density and HF solution. The ideal porosity is 56 % in order to accomodate the change in volume from silicon to oxide and thus to attenuate the strain. The inconveniences are mainly associated with the wet process, relatively large thickness of the Si film (0.5 µm), residual stress, and contamination induced by the chemical process.

2.1.4  Wafer Bonding (WB)

The WB [15] technique provides undamaged crystal quality and more flexibility than SIMOX for both the Si film and the buried oxide layer. There are three basic steps
required for the WB process: (1) mating two silicon wafers at room temperature, (2) annealing the bonded wafers at temperatures above 800 °C for several hours to increase bonding strength, and (3) thinning down one of the two wafers to a proper thickness by grinding and polishing and/or etching.

The main drawback of the wafer bonding technique is its difficulty in producing extremely thin, uniform Si film via the conventional polishing technique. Therefore, the third step is becoming more and more important for manufacturing ultrathin Si films with good uniformity.

2.1.5 Silicon On Sapphire (SOS) & Silicon On Zirconia (SOZ)

The sapphire (alpha-Al$_2$O$_3$) crystals [16] are produced using either the flame-fusion growth technique, Czochralski growth, or edge-defined film-fed growth. The first two of these techniques provide sapphire boules which have to be sliced before polishing, while the third technique provides thin rectangular sapphire ribbons, which have to be cut into circular wafers later on. After mechanical and chemical polishing, the sapphire wafers receive a final hydrogen etching at 1150 °C in an epitaxial reactor, and a silicon film is deposited using pyrolysis of silane at a temperature between 900 and 1000 °C. Due to lattice and thermal mismatch, defect density in these films is quite high, especially in very thin films. The main defects present in the as grown SOS films are: aluminum auto-doping from the Al$_2$O$_3$ substrate and stacking faults. These account for the low values of resistivity, mobility, and lifetime near the interface.

Yttria-stabilized zirconia (YSZ) [17] has been proposed as a substitute for sapphire because of its reduced lattice mismatch and lesser difference in thermal expansion coefficients. The heteroepitaxy of silicon proceeds very similarly in silicon on zirconia and SOS.

2.2 Operation of an SOI MOSFET

The structure of an SOI MOSFET, as shown in figure 2.2 is similar to the conventional bulk MOSFET with the exception that the active silicon layer is separated from the bulk
silicon substrate by a thick buried oxide layer. Thus, the substrate in an SOI MOSFET is electrically floating which gives rise to a number of parasitic effects commonly referred to as floating body effects. These will be discussed in the next chapter.

Depending on the silicon film thickness and the channel doping concentration, three types of SOI MOSFETs can be distinguished. In a thick-film SOI device, fig. 2.3 (B) the silicon film thickness is larger than twice the maximum depletion width, \( x_{d_{\text{max}}} \), which is classically given as:

\[
x_{d_{\text{max}}} = \sqrt{\frac{4\epsilon_s \Phi_F}{qN_A}}
\]  

(2.1)

where \( \Phi_F \) being the fermi potential is given by:

\[
\Phi_F = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)
\]  

(2.2)

As a result, there is no interaction between the depletion zones arising from the front and back interfaces, and a neutral silicon piece, called body exists beneath the front depletion zone. If it is connected to ground via a body contact, the device operation will exactly be like that of a bulk device. However, if the body is left electrically floating, the device will behave like a bulk device, with the exception of floating body effects.
In a thin-film SOI device, fig 2.3 (c), the silicon film thickness is smaller than $x_{d_{\text{max}}}$. The silicon film is fully depleted at threshold, irrespective of the back-gate bias (with the exception of a possible presence of thin accumulation or inversion layers at back interface, if a large negative or positive bias is applied at the back gate, respectively). Among all types of SOI MOSFETs, fully depleted SOI devices with their back interface depleted, exhibit the most attractive properties, such as low electric fields, high transconductance, excellent short channel behaviour and a quasi-ideal subthreshold slope.

Medium thickness SOI device is an intermediate case between thin and thick film device, and is obtained when $x_{d_{\text{max}}} < t_{\text{Si}} < 2x_{d_{\text{max}}}$, $t_{\text{Si}}$ being the film thickness. If the back gate bias causes the front and back depletion zones to coalesce, the device behaves as a thin film device, else it behaves like a thick-film device.

### 2.2.1 Threshold Voltage

For a thick-film SOI device, which essentially behaves like a bulk device due to absence of interaction between the front and back depletion regions, the threshold voltage is same as in a bulk device and is given as:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a x_{d_{\text{max}}}}{C_{ox}}$$

(2.3)
where

\[ V_{FB} \] is the flatband voltage,
\[ \Phi_F \] is the fermi potential, and
\[ x_{d,max} \] is the maximum depletion width.

For a thin-film SOI device, the expressions for threshold voltage as a function of the different possible steady-state charge conditions at the back interface are given as [4]:

\[
V_{th,inv2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\Phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (2.4)
\]

\[
V_{th,depl2} = V_{th,acc2} - \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} (V_{G2} - V_{G2,acc}) \quad (2.5)
\]

\[
V_{th,acc2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{Si}}{C_{ox2}}\right)2\Phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (2.6)
\]

where

\[
C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}},
\]

\[
Q_{depl} = -qN_a t_{Si},
\]

\[
V_{G2,acc} = \Phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} 2\Phi_F - \frac{Q_{depl}}{2C_{ox2}},
\]

\[
V_{G2} = \Phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} \Phi_{s1} + \left(1 + \frac{C_{Si}}{C_{ox2}}\right)\Phi_{s2} - \frac{1}{2} \frac{Q_{depl} + Q_{s2}}{C_{ox2}},
\]

Q_{s2} is the charge in possible back inversion or accumulation layer, \( \Phi_{s1} \) and \( \Phi_{s2} \) being the potentials of front and back silicon/oxide interfaces, \( \Phi_{MS1} \) and \( \Phi_{MS2} \) being front and back work functions respectively.

**2.2.2 Body Effect**

In a bulk device, the body effect is defined as the dependence of the threshold voltage on the substrate bias. In an SOI transistor, it’s similarly defined as the dependence of the threshold voltage on the back-gate bias. In a thick film device, the body effect (or, more aptly back-gate effect) is negligible due to absence of coupling between the front and
back gate. In a thin-film fully depleted device, the body effect parameter, $\gamma$ is obtained from eqn. (2.6),

$$\gamma \equiv \frac{\partial V_{th}}{\partial V_{G2}} = -\frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} \tag{2.7}$$

It can be seen from eqn. (2.7) that the threshold voltage dependence on back-gate bias is linear in case of thin-film SOI transistors.

2.2.3 Output Characteristics

The expression of the current characteristics $I_D(V_{G1}, V_{G2}, V_{DS})$ of a thick-film SOI MOS transistor is identical to that of a bulk MOSFET, with some modifications due to the parasitic bipolar effects coming up due to the presence of an electrically floating body. The derivation of the current characteristics of a thin film, fully depleted SOI device can be done [4] using assumptions of the classical gradual channel approximation [18]. The saturation current in an SOI MOSFET is given as:

$$I_{Dsat} \equiv \frac{1}{2} \frac{W}{L} \mu C_{ox1} (V_{G1} - V_{th})^2 \tag{2.8}$$

where

$$\alpha = \frac{C_{Si}}{C_{ox1}} \text{ for fully depleted device with back interface in accumulation,}$$

$$\alpha = \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} \text{ for fully depleted device with back interface in depletion,}$$

$$\alpha = \frac{\varepsilon Si}{x_{d,max} C_{ox}} \text{ for bulk and partially depleted devices,}$$

Since, $\alpha_{\text{fully depleted SOI}} < \alpha_{\text{bulk}} < \alpha_{\text{back accum SOI}}$, the drain saturation current is highest in the fully depleted device, lower in the bulk device, and even lower in the device with back accumulation. This high saturation current in a thin-film, fully depleted SOI MOSFETs brings about an increase in current drive, which contributes to excellent speed of fully depleted SOI CMOS circuits.
2.2.4 Transconductance

The transconductance of a MOSFET, $g_m$, is a measure of the effectiveness of the control of the drain current by the gate voltage. Transconductance in the case of an SOI MOSFET can be obtained by eqn. (2.8):

$$g_m = \frac{\partial I_{D_S}}{\partial V_{G_1}} = \frac{W\mu_n C_{ox1}}{L(1 + \alpha)} (V_{G_1} - V_{th}) \quad (2.9)$$

Clearly, transconductance follows the same trend as that of drain saturation current with the maximum being for fully depleted SOI device with depleted back interface.

2.2.5 Subthreshold Slope

The subthreshold slope is defined as the inverse of the slope of $I_d(V_g)$ curve in the subthreshold regime, presented on a semilogarithmic model.

$$S = \frac{dV_g}{d(\log I_d)} \quad (2.10)$$

In a thick film SOI device, $S$ is calculated as [4]:

$$S = \frac{kT}{q} \ln(10) \left(1 + \frac{C_D + C_{it1}}{C_{ox1}}\right) \quad (2.11)$$

or,

$$S = \frac{kT}{q} \ln(10) \left(1 + \frac{C_D}{C_{ox1}}\right) \quad (2.12)$$

if the interface traps are neglected.

Here, $C_D$ is depletion capacitance, $C_{it1}$ is the capacitance associated with the charging of the interface traps at the front interface, and $C_{ox1}$ is the front gate oxide capacitance. For a thin-film fully depleted device, $C_D$ is close to zero and neglecting the effect of interface traps, we get

$$S = \frac{kT}{q} \ln(10) \quad (2.13)$$
Therefore, the subthreshold slope of thin-film fully depleted device approaches its theoretical minimum value of 60 mV/decade at room temperature. Thus, these devices exhibit a quasi-ideal subthreshold slope.
Chapter 3

SOI Vs Bulk

In a bulk MOS transistor, only the top region of the silicon wafer is relevant for electron transport. SOI structures emerged from the idea of isolating the active device overlay from the detrimental influence of the underlying silicon substrate by a buried oxide layer. However, this isolation of channel leads to an electrically floating body which leads to some parasitic effects commonly referred to as floating body effects. In this chapter, the various advantages and disadvantages of SOI devices vis-à-vis bulk technologies are discussed.

3.1 Advantages

3.1.1 Dielectric Isolation

SOI circuits consist of single device islands, dielectrically isolated from each other and from the underlying substrate. Because each device sits alone on the top of the insulator, there are no leakage paths to the substrate or to the adjacent devices. This allows both analog and digital devices to be used on the same chip. The inter-device distance is much more shrinkable in SOI than in bulk. The critical limitation of bulk technology for VLSI circuits is due to unavoidable proximity of diffused regions that belong to adjacent components. Sophisticated techniques of trench isolation are necessary in bulk silicon technology to avoid latch-up. Latch-up refers to unintentional activation of parasitic devices. In fig. 3.1 (a), the superposition of PNP and NPN transistors, which share the same diffused regions, is nothing but a thyristor whose turn-on causes uncontrollable high currents and leads to circuit failure. On the other hand, SOI is naturally free from latch-up problem.
3.1.2 Vertical Junctions

In regular SOI films, the source and drain regions extend to the insulator, and only their lateral sides serve as junctions, as it can be seen from fig. 3.1 (b). The surface of such a junction is much smaller than in bulk silicon. This smaller surface yields a substantial reduction in parasitic capacitances, and hence in propagation delays and dynamic power consumption. In short, for predefined power consumption, much denser and faster circuits can be integrated on SOI wafers.

3.1.3 Short Channel Effects

In small geometry MOS transistors, the depletion zones induced by the source and drain junction become relatively significant and impede the gate control over the whole space charge region. A number of small channel effects like threshold voltage roll-off, degradation of subthreshold slope, drain induced barrier lowering, punch-through etc. originate due to the “charge sharing” between gate and junctions. SOI devices are more immune to short-channel effects [20]. Basically, the extension of source/drain depletion regions is restricted by the junction size and the dual gate control (via front-gate and silicon substrate) of the surface potential.

3.1.4 Reliability

The primary motivation for developing SOI technologies was their excellent tolerance of transient radiation effects. Incoming particles generate electron-hole pairs in proportion to the device volume. Resulting photocurrents acts as leakage currents, causing charge.
collection and soft errors. This gets dramatically reduced in SOI as the volume exposed to carrier generation is 2-3 orders of magnitude smaller than in bulk Si, due to the presence of buried oxide layer in these devices. Also, when ionizing radiation travels through a transistor, it creates a tail of mobile charge particles on its wake which increase with the path length of the radiation. The buried insulator layer lessens the amount of mobile charge that is generated, since mobile charges can’t be created there.

3.2 Disadvantages

3.2.1 Self Heating Effects

Due to thermal isolation of substrate by the buried insulator in an SOI transistor, removal of excess heat generated by the Joule effect within the device is less efficient than in bulk, which leads to substantial elevation of device temperature. The excess heat mainly diffuses vertically through the buried oxide and laterally through the silicon island into the contacts and metallization. Due to the relatively low thermal conductivity of the buried oxide, the device heats up to 50 to 150 °C. This increase in device temperature leads to a reduction in mobility and current drive, thus degrading the device performance over a period of time.

3.2.2 Floating Body and Parasitic Bipolar Effects

![Parasitic bipolar transistor of the SOI MOSFET](image)

**Fig. 3.2:** Parasitic bipolar transistor of the SOI MOSFET
The presence of a floating volume of silicon beneath the gate is at the origin of several effects unique to SOI, generically referred to as floating body effects [21]. There exists a parasitic bipolar transistor in the MOS structure. If we consider an n-channel device, the N⁺ source, the P-type body and the N⁺ drain indeed form the emitter, the base, and the collector of an NPN bipolar transistor, respectively. In a bulk device, the base of the bipolar transistor is usually grounded by means of a substrate contact. But, due to the floating body in an SOI transistor, the base of the bipolar transistors is electrically floating. This parasitic bipolar transistor (fig.3.2) is origin of several undesirable effects in SOI devices.

Next, we discuss some important floating body and parasitic bipolar effects in SOI devices.

### 3.2.2.1 Kink Effect

The kink effect consists into the appearance of a kink in the output characteristics of an SOI MOSFET working in strong inversion, as shown in fig. 4.12 (b). The kink is very strong in n-channel transistors but, is usually absent from p-channel devices.

Let us consider a thick-film, partially depleted SOI n-channel transistor. When the drain voltage is high enough, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs, due to an impact ionization mechanism. The generated electrons move into the channel and the drain, whereas the holes, which are majority carriers in the p-type body, migrate towards the place of lowest potential i.e., the floating body.

The injection of holes into the floating body forward biases the source-body diode. The floating body reaches a positive potential, as given by the following equation [4]:

\[
I_{\text{holes,gen}} = I_{S0} \left( \exp \left( \frac{qV_{BS}}{nkT} \right) - 1 \right)
\]  

(3.1)

where \( I_{\text{holes,gen}} \) is the hole current generated near the drain,

\( I_{S0} \) is the saturation current of the source-body diode,
$V_{BS}$ is the potential of the floating body, and, 
n is the ideality factor of the diode.

The increase of body potential gives rise to lowering of threshold voltage and source-body potential barrier. More minority carriers are able to flow from source to the channel, thereby causing an excess drain current and producing many more pairs through the avalanche process. This positive feedback results in a sudden increase in $I_D$ or “kink” in output characteristics. If the minority carrier lifetime in the silicon film is high enough, the kink effect can be reinforced by the NPN bipolar transistor (fig. 3.2). The “base” hole current is amplified by the bipolar gain, which gives rise to an increased net drain current, sometimes referred to as second kink [19].

Now, let us consider the case of a thin-film, fully depleted SOI n-channel MOSFET. It has been shown [22] that the electric field near the drain is lower in the fully depleted device than in partially depleted one. As a result, less electron-hole pair generation takes place in the fully depleted device. Also, contrary to the case of a partially depleted transistor, the source-to-body diode is “already forward biased” due to the full depletion of the film, and therefore, holes can readily combine in the source without having to raise the body potential there. This explains why thin film fully depleted n-channel MOSFETs are free of kink effect.

![Fig 3.3: Potential in neutral region from source to drain in PD and FD SOI Devices](image)

The p-channel devices are free of kink effect because coefficient of electron-hole pair generation by energetic holes is much lower than that by energetic electrons. The kink effect is not observed in bulk devices as the majority carriers generated by impact
ionization can escape into the substrate or to a well contact. The kink effect can be eliminated from the partially depleted SOI MOSFETs if a body contact is provided for removal of excess majority carriers from the device body.

### 3.2.2.2 Anomalous Subthreshold Slope and Single Transistor Latchup

If the drain voltage is high enough, impact ionization can occur even in the subthreshold region, even though the drain current is very small. When the device is off, there is no impact ionization, and the body potential is equal to zero, since there is no base to source current. When the gate voltage is increased, the weak inversion current can induce impact ionization in the high electric field region near the drain, holes are generated, the body potential increases, and the threshold voltage gets reduced. Consequently, the whole $I_D(V_{GS})$ characteristic shifts to the left, and the current can increase with gate voltage with a slope larger than 60 mV/decade. In other words, subthreshold slopes lower than the theoretical limit of 60 mV/decade can be observed [22].

\[
\Delta I_D = \beta (M-1) I_{ch}
\]

where $I_{ch}$ is the channel current (fig. 3.2). This increase of drain current constitutes a positive feedback loop on the current flowing in through the device:

Fig. 3.4: Illustration of a single transistor latch: (a) “Normal” subthreshold Slope at low drain voltage, (b) Device latch up at higher drain voltage

If the minority carrier lifetime in the silicon film is high enough, the parasitic bipolar transistor can amplify the base current constituted by hole current generated by impact ionization near the drain. The resulting increase of drain current is given by $\Delta I_D=\beta (M-1) I_{ch}$ where $I_{ch}$ is the channel current (fig. 3.2).
the drain current suddenly increases, and an infinite subthreshold slope is observed (fig. 3.3). This phenomenon is called “single transistor latch-up”. If the drain bias is large enough, the positive feedback loop cannot be turned off once it has been triggered. Therefore, the device remains on even when gate voltage is negative.

The floating body effects coupled with parasitic bipolar transistor pose a major obstacle which need to be overcome before SOI can be used for practical applications. There are two main approaches. One involves source engineering like lightly doped source (LDS) [21], gate overlapped LDD structure [23], dual source SOI MOSFET [24], delta doped [25] and narrow bandgap [26] source structures, bipolar embedded source structure (BESS) [27] and, Ar-ion implantation technique [28]. The other approach is the body contact method to fix the body potential like field shield technique [29].
Chapter 4

Characterization and Simulation Results on SOI MOSFETs

Experiments were performed on conventional and LAC SOI MOSFETs in order to compare their performances. The experiments were conducted on SIMOX wafers having silicon film thickness of 35 nm. The same wafer contained both conventional and linear asymmetric channel devices. The experiments were performed on devices having width of 10 µm and channel lengths varying from 0.1 µm to 1 µm. The first part of experiments involved study of effects of back gate bias on front gate. These include front gate threshold voltage and subthreshold voltage variation with back gate bias. Back gate transfer characteristics have also been obtained. The second part of experiments comprised of comparing the device performance of conventional and LAC SOI MOSFETs by studying $V_{th}$ roll-off, DIBL, and transfer and output characteristics.

The second section discusses the simulations performed on these devices using the process simulator, TSUPREM-4 [30] and device simulator, Medici [31]. The purpose of doing simulations was to get an overall understanding of the working of these devices. The approach was to first match the simulations with experimental characteristics and then, gain a deeper insight into the working of these devices by studying variations in various parameters and physical quantities under different biasing conditions. Simulations have been performed on LAC and conventional SOI devices and the advantage of LAC over conventional devices has been investigated.

Only simulations of very basic flavour were possible during the project as the emphasis shifted to characterization from second stage onwards. The simulations could be performed only during the first stage of the project.
4.1 Electrical Characterization of SOI MOSFETs

The process sequence details of the devices used are illustrated in following table:

<table>
<thead>
<tr>
<th>Para.</th>
<th>Conventional</th>
<th>Asymmetric</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tox</td>
<td>JVD oxide, 3.1 nm EOT</td>
<td></td>
</tr>
<tr>
<td>TSOI</td>
<td>35 nm</td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td>BF$_2$, 40 keV, 8e12 cm$^{-2}$</td>
<td>BF$_2$, 25 keV, 2e13 cm$^{-2}$, Tilt=10</td>
</tr>
<tr>
<td>S/D ext.</td>
<td>As, 10 keV, 2e14 cm$^{-2}$</td>
<td>As, 40 keV, 5e15 cm$^{-2}$</td>
</tr>
<tr>
<td>DP S/D</td>
<td>Ge, 20 keV, 1e15 cm$^{-2}$, tilt=0</td>
<td></td>
</tr>
</tbody>
</table>

Both conventional homogeneously doped channel SOI nMOSFETs and LAC SOI nMOSFETs are fabricated on the same wafer for fair comparison. The threshold voltage adjustment of the conventional SOI nMOSFETs is done before the gate oxidation while that of the LAC nMOSFETs is done after the gate formation implanted at a tilt angle of 10°. E-beam lithography is used to define the gate. Jet Vapor Deposited (JVD) nitride having an equivalent oxide thickness (EOT) of 3.1 nm has been used as gate dielectric. The thickness of the SOI film is 35 nm. A two-step titanium silicidation process with Ge pre-amorphization is implemented to control the silicide depth and reduce the series resistance. The first step anneal is 450 °C, 3 min followed by a selective etch to remove TiN and unreacted Ti. The second step is 780 °C, 30 seconds. Such a low temperature silicidation reduces the dopant redistribution which is important to realize asymmetric channel profiles in deep sub-micrometer regime.

4.1.1 Back Gate Characterization

The dual-gate configuration of SOI MOSFETs offers various biasing options, independent or simultaneous biasing of the two interfaces. In thick, partially depleted films, triggering both channels at once results in the total current being simply the parallel combination of the two individual contributions. However, the intrinsic properties of the front channel are not modified by the back bias. However, in thin film fully depleted
devices, this interface coupling leads to variation in threshold voltage, subthreshold slopes and other front gate parameters with back gate bias variation.

It can be seen that the front gate threshold voltage depends on the back gate bias. When the back gate is in accumulation, the threshold voltage variation is lower as compared to the case when it is in depletion. This corroborates the fact that interface coupling takes place when either of the interfaces is depleted. Also, the rate of change of threshold voltage for identical change in back bias in LAC devices is much smaller than that in conventional device.

Fig 4.1: Front gate threshold voltage variation with back gate bias for (a) conventional and (b) LAC SOI nMOSFET

Fig 4.2: Back gate transfer characteristics for (a) conventional, and (b) LAC SOI device
Fig 4.2 (a) and (b) show the back gate transfer characteristics of conventional and LAC SOI nMOSFET with the front gate in accumulation to decouple the front gate from the back gate. The back gate threshold voltage for LAC SOI device is higher than that for the conventional SOI. This shows that the off state leakage current of back gate is lower in the LAC SOI nMOSFET. The current levels are also lower in the case of LAC devices. This can be attributed to the higher threshold voltages in LAC devices than conventional SOI devices.

![Graph showing back gate transfer characteristics](image)

**Fig 4.3:** Subthreshold voltage variation with channel length for (a) conventional and (b) LAC SOI nMOSFET as a function of drain bias

For low power high performance devices, the subthreshold slopes must be close to theoretical limits. Due to the presence of buried oxide in SOI devices, quasi-ideal subthreshold slopes can be obtained as discussed in section 2.2.5. Fig. 4.3 (a) and (b) shows the subthreshold slopes for conventional and LAC SOI devices. The back gate is kept in accumulation.

From the graphs, we observe that both devices exhibit high subthreshold slopes for low channel lengths and S decreases as the channel length decreases. In case of LAC devices, the values keep on decreasing till channel lengths of the order of 0.5 µm whereas in the case of conventional devices, the values start increasing again around channel lengths of 0.25 µm. Also, the drain bias dependence is less pronounced in the case of LAC devices.
4.1.2 Threshold Voltage Roll-off and Drain Induced Barrier Lowering

The threshold voltages decrease drastically as the channel lengths are scaled down to sub micron regimes. This phenomenon is known as $V_{th}$ roll off. It occurs due to the fact that as channel lengths decrease, the charge controlled by the gate is shared by source and drain, which weakens the control of gate. In long channel devices, the effect of drain voltage on the threshold voltage is not appreciable. However, for short channel devices, a sufficiently large drain bias can lower the lowering of barrier near source end. This phenomenon is referred to as Drain Induced Barrier Lowering (DIBL).

![Fig. 4.4](image1.png)  
**Fig. 4.4:** Threshold Voltage roll-off in conv and bulk SOI MOSFETs

![Fig. 4.5](image2.png)  
**Fig. 4.5:** Drain Induced Barrier Lowering in conv and bulk SOI MOSFETs

Fig. 4.4 and 4.5 show $V_{th}$ roll off and DIBL characteristics in SOI MOSFETs respectively. The conventional SOI MOSFETs display little $V_{th}$ roll off as the decrease in threshold voltage becomes appreciable only at channel lengths less than 0.25 $\mu$m. On the other hand, inverse $V_{th}$ roll off (roll up) is observed for LAC SOI MOSFETs. This $V_{th}$ roll up may be explained as follows. In short channel LAC SOI MOSFETs, the average doping in the channel increases due to the tilt angle $V_{th}$ adjust implant in these devices. This increased doping leads to an increase in threshold voltage for small channel LAC SOI MOSFETs.

Drain induced barrier lowering has been estimated by calculating the change in threshold voltage for one volt change in drain bias using the transfer characteristics at drain biases of 0.1 and 0.2 V. DIBL is found to be very small for channel lengths more
than 0.5 µm. For devices smaller than 0.5 µm, the LAC devices show less DIBL as compared to the uniform devices. This can be attributed to the heavy doping near the source region in these devices, which causes the barrier to be higher and thus, making these devices less likely to be affected by changes in drain bias.

4.1.3 Transfer Characteristics

Fig. 4.6 shows the transfer characteristics obtained for conventional and LAC SOI MOSFETs. Fig. 4.6 (a) and (b) show the characteristics for both devices with the back gate in accumulation and depletion, respectively. It can be clearly seen that the transfer characteristics of LAC device don’t shift as much as that of conventional devices with similar back gate biasing. This exhibits lesser control of back gate in the front channel conduction in LAC devices. Fig 4.6 (c) shows the transfer characteristics obtained for various drain biases. The back gate has been grounded for this experiment. The plots have
been scaled by the corresponding threshold voltages in order to give a clear idea. It can be seen from the graph that the LAC SOI devices exhibit larger transconductance than their conventional counterparts. This may be attributed to the reduction in the scattering centres near the drain end where peak electric field lies and also due to early velocity overshoot taking place near the source region.

### 4.1.4 Output Characteristics

Fig. 4.7 (a) and (b) shows the output characteristics obtained for LAC and conventional SOI devices. LAC SOI MOSFET exhibits a faint kink at drain bias of 0.8 V. On the other hand, conventional device doesn’t show any kink. This implies that the LAC device is operating in the partial depletion mode at this voltage bias whereas the conventional device is operating in full depletion mode under the present biasing conditions.

### 4.2 Simulation of SOI MOSFETs

Some basic simulations were performed during the first stage of this project. However, during the second and final stages, the emphasis shifted to characterization and not much work in simulations could be done. In the simulations, the basic approach has been to understand LAC devices in order to study their performance vis-à-vis conventional devices. From the process sequence available, devices were simulated using the process
simulator TSUPREM-4, and then device simulator Medici was invoked which reads in the device files generated via TSUPREM-4.

4.1.1 Process Sequence for LAC and conventional SOI nMOSFETs

The devices simulated have channel lengths of 0.1 \( \mu \text{m} \) and silicon film thickness of 35 nm. The buried oxide thickness is 180 nm. Both the conventional and LAC devices are LDD devices. For this purpose, a sidewall spacer of 100 nm has been used. The process sequence for LAC devices is as follows:

1. Start with a p-type SIMOX wafer.
2. Perform oxidation to form gate oxide.
3. Deposit poly and define the gate.
4. Do a tilt angle implant for \( V_{th} \) adjustment.
5. Do implantation of light dose of n-type (LDD implant).
6. Form sidewall spacers.
7. Do implantation of heavy dose of n-type (Source/Drain implant).
8. Anneal to activate the implants.
9. Pattern source and drain, and define the metal contacts.

The process sequence for conventional devices is identical but for \( V_{th} \) implant, which in these devices is done after step 1 \( i.e. \) before forming gate oxide. However, the actual fabrication of SOI involves high energy implantation of oxygen in silicon wafer and recrystallization of the top silicon layer. TSUPREM-4 can not simulate this process. For the purpose of simulation, silicon film has been epitaxially grown on top of oxide.

The process details of the devices are given in following table:

<table>
<thead>
<tr>
<th>Para.</th>
<th>Conventional</th>
<th>Asymmetric</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tox/Teff</td>
<td>39 A (Dry 800 C, 20 min Oxi, 950 C, 20 min anl)</td>
<td>35 nm</td>
</tr>
<tr>
<td>TSOI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{th} )</td>
<td>BF2, 25KeV, 5E12 ( \text{cm}^{-2} )</td>
<td>BF2, 25KeV, 6E13 ( \text{cm}^{-2} ), Tilt=7</td>
</tr>
<tr>
<td>S/D ext.</td>
<td>As, 10 keV, 2E14 ( \text{cm}^{-2} )</td>
<td></td>
</tr>
<tr>
<td>DP S/D</td>
<td>As, 40 keV, 5E15 ( \text{cm}^{-2} )</td>
<td></td>
</tr>
</tbody>
</table>
4.2.2 Simulation Details and Results

![Simulation Diagram](image)

The device was made using process simulator, TSUPREM-4. The mesh was made dense in the channel and source/drain regions by optimizing the gridlines spacing and eliminating columns. The final mesh structure obtained is shown in fig. 4.9. As
mentioned above, since, TSUPREM-4 can't simulate the SIMOX process, the problem was overcome by using REGION statement. By using this statement, one can specify the material type of a mesh region. Gate oxide was grown at 800 °C in dry oxygen ambient and annealed in nitrogen gas ambient. The oxide thickness extracted using the simulator was 3.2 nm as against 3.9 nm reported in the process sequence file. It may be attributed to non-specification of all the parameters in the diffusion step while simulating. The other process steps were carried out in accordance with the process sequence as mentioned above. After, deep source/drain implant, the device was subjected to Rapid Thermal Anneal (RTA) by annealing it at a temperature of 1020 °C for 15 seconds. Next, the source/drain was patterned and metal was deposited. The final structure obtained is shown in fig 4.10.

![Active Boron and Arsenic profiles for (a) conventional, and (b) LAC SOI device](image)

**Fig 4.11:** Active Boron and Arsenic profiles for (a) conventional, and (b) LAC SOI device

Fig 4.11 (a) and (b) show the plots of active boron and arsenic concentrations for the conventional and LAC SOI devices. The active arsenic profile is same in both the devices whereas the active boron profile is different, due to the difference in \(V_{th}\) adjustment implant schemes in the two devices. Since, in conventional device, this implant is done before depositing the gate oxide, it is uniform across the channel, whereas in LAC devices, it is done after depositing the gate oxide and with a tilt. This causes the doping in the channel to be higher on the source as compared to that on drain side. Fig 4.11 (b) clearly shows more heavily doped channel in the source side than the drain side. The final device structure was saved in a format, which the device simulator Medici could read directly. The device was simulated and the simulated results were matched with the
experimental data by fine tuning various default values in the simulator. It was observed that the threshold voltages differed by a small quantity. The threshold voltage matching was done by adjusting the dose and energy by small values.

After matching the threshold voltages, the actual characteristics were matched by perturbing the default values of parameters associated with mobility, etc. Various relevant models were turned on in the simulator to account for the short channel effects like vertical field dependent mobility model, and other such relevant models. The simulation of output characteristics proved to be an arduous task. Since, the body is floating in these devices, impact ionization takes place near the drain region. To account for this, models specifying carrier generation due to impact ionization were included in the simulation. However, when simulations were performed, the problems of non-convergence of solutions arose.

To get around this problem, energy balance equations based on hydrodynamic model were used. Local carrier heating in high and spatial, rapidly varying electric fields is modeled using a self-consistent solution of the drift-diffusion and carrier energy balance equations. However, with the inclusion of these models, still the problem of convergence was not totally resolved. The solutions were converging for only a few bias points forcing to look for alternative modes of solution.

To address this difficulty, it was decided to change a few parameters of the solver algorithm. After spending much time on the many parameters available in the Newton’s solver scheme, finally changing two parameters namely STACK and ITLIMIT achieved the convergence at all the bias points. ITLIMIT refers to the parameter specifying the maximum number of Newton iterations at a given bias point. The default value is 20, which was inadequate for these simulations. It was increased to 50. STACK refers to the maximum number of times the solver tries to converge to a solution by halving the bias parameter. The default value is 4. But, it was found that this stack size was not enough for the simulations being performed. It was increased to 10, which is the maximum allowed value of this parameter.  

Fig. 4.12 (a) and (b) show the transfer and output characteristics obtained for these devices, respectively.
LAC SOI devices exhibit higher transconductance than conventional SOI devices and kink in the output characteristics is also observed in these devices. It shall be noted that, as discussed in section 4.1.4, LAC devices are operating in partially depleted mode while the conventional devices are operating in the fully depleted mode. The simulations confirm this observation. Also, it can be seen from the output characteristics that LAC devices have higher drive currents and higher breakdown voltages. Also, a better saturation behavior is observed in LAC devices where as a clear non-saturation behavior can be seen for conventional devices. This is mainly due to the improved short-channel performance of LAC MOSFETs.

Fig 4.12: Simulated (a) transfer and (b) output characteristics for conv and LAC SOI devices
Chapter 5

Gate Induced Drain Leakage (GIDL) Studies on SOI MOSFETs

Minimization of off-state leakage currents is an important issue in high-density, very low power, battery powered CMOS technologies. The off-state Gate-Induced-Drain-Leakage (GIDL) current, caused by band-to-band tunneling in the gate-drain overlap region, therefore, assumes greater significance. Due to the parasitic bipolar action in the floating body, the GIDL current is found to be substantially enhanced in a short-channel SOI MOSFET as compared with bulk devices [32].

The lateral bipolar transistor effects are very important for understanding of breakdown mechanisms in SOI MOSFETs. It is, thus, desirable to be able to measure the lateral bipolar transistor current gain, $\beta$ in SOI MOSFETs. A technique based on GIDL current enhancement in short channel MOSFETs has been implemented for this purpose.

5.1 GIDL Basics

In an n-MOSFET when the gate potential is very low or negative, in which case the front channel is off or in accumulation and a high drain potential is applied, tunneling current flows from drain to substrate. Since this is a form of undesired leakage current caused at low gate voltages, it is referred to as Gate Induced Leakage Current (GIDL). Referring to fig. 5.1, this leakage current for negative bias is due to tunneling current in the deep depletion region. In this gate-to-drain overlap region, the tunneling of valence-band electrons into the conduction band generates electron-hole pairs. This occurs because of the high vertical electric field in the gate-drain overlap region. Fig. 5.2 shows band diagram near the gate-to-drain overlap region at high drain voltage and device in the off state or in accumulation.
The GIDL current due to Band-to-Band tunneling follows the relationship given as [18]:

$$I_D = AE_S \exp\left(-\frac{B}{E_S}\right)$$  \hspace{1cm} (5.1)

where $A$ is a constant and $B$ equals about 21.3 MV/cm. $E_S$ can be expressed as

$$E_S = \frac{V_{DG} - V_{SURF}}{3T_{ox}}$$  \hspace{1cm} (5.2)

where $V_{DG} = (V_D - V_G)$. $V_{SURF}$ is the surface potential of the depleted region at the onset of B-B tunneling and is equal to 1.2 volts.

Due to the vertical field present in the overlap region, these electrons and holes are collected by the drain and substrate, respectively. As the gate voltage is made more negative or the drain potential is increased, the vertical field increases leading to an increase in GIDL leakage current. Reduction in current is observed for LDD devices under GIDL bias. This may be attributed to reduction in the electric field in the gate-drain overlap region. GIDL has been used earlier to characterize interface traps and later on to measure oxide charge trapping using GIDL transients [36].

### 5.2 GIDL in SOI MOSFETs

The origin of GIDL remains identical even in the case of SOI MOSFETs [32] as in the case of bulk MOSFETs. The front channel in the device is kept in off state or in accumulation. Fig. 5.3 shows the schematic diagram of current flow in an SOI n-channel MOSFET in GIDL mode with the front channel turned off.
The high electric field in the gate-drain overlap region causes electron tunneling from valence band to conduction band. The electrons, as in the case of bulk device, move out from the drain. However, the holes, unlike in bulk device, cannot flow out to the substrate due to the buried oxide present. As a result, the holes flow to the floating body and forward bias the source-body junction. This junction is the emitter-base junction of the parasitic bipolar junction transistor. The GIDL current, thus, serves as the base current for the lateral parasitic bipolar transistor as shown in fig. 5.4. This GIDL current, which is independent of the channel length, is amplified by the gain of the lateral BJT. The resultant current at the drain is thus given as:

$$I_D = \beta I_{GIDL} + I_{GIDL} = (\beta + 1)I_{GIDL}$$

(5.3)

where $\beta$ is the gain of the lateral BJT.

The current gain of the lateral BJT increases as the base width decreases. Therefore, for short channel devices, $\beta$ becomes significant, which is not the case with long channel devices. Thus, the GIDL current gives a method for extraction of $\beta$ for an SOI device. By finding the ratio of drain currents of a short channel device and long channel device operating under GIDL bias, the value of $\beta$ can be easily extracted. It is readily applicable to SOI devices, as it does not require a body contact.
5.3 Results Obtained

Experiments were performed on bulk MOSFETs, conventional and linear asymmetric channel SOI MOSFETs in order to study the GIDL currents in these devices.

5.3.1 Effect of variation of gate voltage on GIDL currents

Fig 5.5 shows the variation of GIDL current with change in applied gate voltage. As the applied gate voltage $V_G$ increases, the vertical field in the gate-drain overlap region increases. This leads to an increase in the band-to-band tunneling current. Since the base current increases, the resultant off-state leakage current also increases. The results have been plotted for a LAC SOI MOSFET. Similar trends were noted for bulk and conventional SOI MOSFET also.

5.3.2 GIDL Currents in bulk MOSFETs

The GIDL currents were first studied for bulk MOSFETs. The devices used in the experiments had channel lengths of 10 µm, 5 µm, 1 µm and 0.25 µm. A GIDL bias of -1.0 Volt was applied and drain voltage was swept from 0 to 3 Volts. The GIDL currents measured for different channel lengths are shown in fig. 5.6. The GIDL current was more or less constant with respect to the channel length. This indicates the validity of the statement that GIDL remains constant with varying channel lengths.
It can be explained by the fact that band-to-band tunneling depends on $V_{DG}$ and hence, is independent of channel length. Also, since the holes flow into the substrate, there is no parasitic bipolar action in bulk MOSFET. Thus, GIDL current remains constant with respect to channel length in bulk MOSFETs and no enhancement of GIDL current is observed in these devices.

5.3.3 GIDL Currents in conventional SOI MOSFETs

GIDL experiments were performed to estimate the gain of parasitic lateral bipolar transistor present in the conventional SOI MOSFET. The devices used had channel lengths 10 $\mu$m, 5 $\mu$m, 1 $\mu$m and 0.25 $\mu$m. The gate oxide thickness and the channel width were 3.9 nm and 20 $\mu$m, respectively. A GIDL bias of -1.0 Volt was applied and the drain voltage was varied. The drain currents measured for different channel lengths are shown in fig. 5.7.

As the channel length decreases, the off-state leakage current increases. For devices of lengths 10 $\mu$m and 5 $\mu$m, currents are low due to absence of lateral BJT gain $\beta$. As the channel length decreases, the base width of the lateral parasitic bipolar transistor also decreases causing the current gain, $\beta$ to increase. Hence, the GIDL current is amplified and is higher than that for long-channel devices. This can be seen for devices of lengths 1 $\mu$m and 0.25 $\mu$m in which currents are high due to the presence of amplification factor.
Comparing the devices of lengths 10 \( \mu \text{m} \) and 0.25 \( \mu \text{m} \), we see that for low \( V_D \), the drain currents are equal. This is because \( \beta \) is very small at very low collector current levels. The current gain \( \beta \) increases with increasing collector current level. The value of \( \beta \) is obtained using equation (5.3), assuming that \( I_{\text{GIDL}} \) is constant with respect to channel length. This was proved in the earlier section using the GIDL currents present in bulk MOSFETs. For \( V_D = 2.75 \) Volts, the value of \( \beta \) is 28.75 for \( L = 0.25 \mu \text{m} \) device and for \( L = 1 \mu \text{m} \) device, \( \beta \) is 1.52. Thus, the value of \( \beta \) increases with decrease in channel length and the resultant enhancement of off-state gate-induced-drain-leakage current becomes significant for short channel conventional SOI MOSFETs.

5.3.4 GIDL Currents in Lateral Asymmetric Channel SOI MOSFETs

LAC SOI devices tend to offset the harmful floating body and parasitic bipolar transistor effects by reducing the drain field and thus impact ionization [34]. In addition to that, LAC devices also prevent short channel effects like \( V_{TH} \) roll-off, DIBL and reliability issues like hot carrier effects. LAC SOI MOSFETs, therefore, promise many advantages over conventional SOI MOSFETs [4,5]. It thus becomes necessary to characterize the floating body effects in LAC SOI MOSFET to prove its advantages vis-à-vis conventional SOI MOSFETs.

In order to determine the efficacy of LAC SOI in reducing the parasitic bipolar action, GIDL current studies were also performed on them. The devices used had channel lengths of 10 \( \mu \text{m} \), 5 \( \mu \text{m} \), 1 \( \mu \text{m} \) and 0.25 \( \mu \text{m} \). GIDL bias of -1.0 Volt was applied and drain voltage was varied. Fig. 5.8 shows the off-state leakage current trends in LAC SOI MOSFET. Lateral parasitic bipolar gain was calculated using equation (5.3). The value of \( \beta \) for \( L = 0.25 \mu \text{m} \) device is 5.6 and for the \( L = 1 \mu \text{m} \) device, it is equal to 2.0. This measured value of \( \beta \) is one order of magnitude lower than that of conventional SOI MOSFET. As the length of the device decreases, the effectiveness of lateral asymmetric channel doping increases. It thus shows that the LAC SOI MOSFET shows immense promise towards reduction of \( \beta \) of the lateral parasitic bipolar transistor and thus, in minimization of floating body effects.
Fig. 5.9 shows the output characteristics for conventional and LAC-SOI MOSFETs. Besides higher drain currents due to the higher average carrier velocity in the channel, a reduction in floating body effects is evident in LAC SOI MOSFETs as can be seen from the delayed appearance of kink. This can be explained by the lower lateral electric field near the drain region as compared to conventional SOI MOSFETs. Fig. 5.10 shows the lateral electric field variation along the channel for conventional and LAC SOI MOSFETs obtained from Medici [31] simulations. The lower peak lateral electric field for LAC SOI MOSFET is due to a lower doping near the drain side of the channel. This leads to lower impact-ionization and hence lower hole generation, which results in a delayed kink in the drain current characteristics.

For shorter channel devices, the peak electric field reduction near the drain in LAC SOI devices becomes significant leading to a lower parasitic bipolar gain compared to the conventional SOI devices. The wider junction depletion region and the lower field across the junction in LAC MOSFETs results in reduced band-to-band tunneling giving rise to a lower hole current. As $\beta$ is known to depend strongly on the parasitic bipolar collector current levels [34], the parasitic action is suppressed in LAC SOI, as can be seen from an order of magnitude lower GIDL currents observed in LAC SOI MOSFETs. Also, due to higher doping in channel region near source, there exists a field which impedes the flow of carriers causing the emitter injection efficiency of the parasitic bipolar junction
transistor to decrease. This leads to lessening of the current gain, $\beta$. Thus, channel engineering is an effective way to alleviate the floating body effects in deep sub-micron SOI MOSFETs, where the second order effects like GIDL currents cannot be neglected due to the parasitic bipolar action.

5.4 Conclusions

The enhancement of off-state gate-induced drain leakage current is significant for short-channel SOI MOSFETs. The parasitic bipolar current gain values for uniform and LAC SOI MOSFETs have been experimentally evaluated using GIDL current technique. LAC SOI MOSFETs have been shown to give rise to reduced floating body effects as a result of lower electric field in the gate-drain overlap region. The extracted parasitic bipolar gain values are an order of magnitude lower for the LAC SOI MOSFETs as compared to the conventional SOI MOSFETs.

This technique can also be used for hot carrier analysis in SOI MOSFETs [35]. Significant changes in off-state gate-induced-leakage current as a result of the channel hot-carrier stress in short channel SOI nMOSFETs are observed. Similar mechanism as discussed above is at work. By hot carrier stress, electron hole pairs are produced and parasitic bipolar transistor turns on leading to enhancement of GIDL currents. Moreover, GIDL current transients have been used to investigate oxide charge trapping and detrapping in a hot carrier stressed nMOSFET [36]. This technique is based on the principle that the silicon surface field and thus GIDL currents vary with oxide trapped charge. This can be adapted to SOI devices and by monitoring the temporal evolution of GIDL currents, the oxide charge trapping/detrapping characteristics can be obtained.
Chapter 6

Multi Frequency Transconductance Technique for Interface State Characterization

Interface characterization is of paramount importance in reliability studies of small geometry MOSFETs with novel gate dielectric. However, most of the techniques developed for characterizing bulk Si MOSFETs [6-9] cannot be used for modern SOI devices, which have complex dielectrics and small geometry. This is because there is no substrate contact available in these devices. Interface characterization, using the multi frequency transconductance technique, has been done previously with an HP 4192A impedance analyzer on bulk MOSFETs [9] and long channel SOI MOSFETs [38]. However, this measurement configuration cannot be used in short-channel devices because it is difficult to eliminate the effects of parasitics and gate leakage currents. The technique has been implemented using a lock-in-amplifier and validated by charge pumping measurements on bulk devices.

Jet-Vapor-Deposited (JVD) nitrides have excellent electrical properties as gate dielectric in terms of lower gate leakage and competitive transconductance, drain current drive and interface quality compared to thermal SiO$_2$ [10]. Detailed electrical characterization of sub100 nm bulk MNSFETs has also been reported with JVD silicon nitride as gate dielectric [11]. Hot carrier degradation effects (HCE) are observed in short-channel MOSFETs because of the high electric field due to which there is carrier heating, and are especially of concern for new dielectrics with small band-edge discontinuities at the interface. Detailed hot carrier stress studies have been performed using the multi-frequency transconductance technique on SOI JVD MNSFETs to address this area of concern.


### 6.1 Multi Frequency Transconductance Technique Details

The transconductance of an MOSFET biased in weak inversion is given by [9]:

\[
g_m = \frac{I_d}{(kT/q)} \frac{C_{ox}}{C_{ox} + C_d + C_{inv} + Y_{it}/j\omega} \tag{6.1}
\]

where

- \( C_d \) is the depletion capacitance,
- \( C_{ox} \) is the gate oxide capacitance,
- \( Y_{it} \) is the interface state admittance,
- \( C_{inv} \) is the inversion-channel capacitance, and,
- \( \omega \) is the angular frequency of applied gate signal.

For \( \omega = 0 \), \( Y_{it} = j\omega C_{it} \), where \( C_{it} \) is the static capacitance of interface traps, so that the real part of the inverse static transconductance can be expressed as:

\[
\text{Re}\left\{\frac{1}{g_m} \right\} = \left(\frac{kT/q}{I_D}\right) \frac{C_{ox} + C_d + C_{inv} + C_d}{C_{ox}} \tag{6.2}
\]

Interface traps, which respond to gate excitation at low frequencies, are unable to do so at high frequencies, since the trapping and detrapping cannot follow the excitation. Therefore, the contribution from interface traps to the capacitance becomes zero and the real part of the inverse high-frequency transconductance is given by:

\[
\text{Re}\left\{\frac{1}{g_m} \right\} = \left(\frac{kT/q}{I_D}\right) \frac{C_{ox} + C_d + C_{inv}}{C_{ox}} \tag{6.3}
\]

It has been shown [19] that for MOSFETs with channel lengths smaller than 10 \( \mu \)m and operating in weak inversion regime, the phase shift due to lateral transport of inversion carriers can be neglected up to frequencies much larger than at which the interface traps become totally inactive as for such a MOSFET, the delay in build up of inversion layer is negligible. Therefore, \( C_{inv} \) can be taken to be independent of the ac signal applied at gate and equations (6.2) and (6.3) allow us to express \( C_{it} \) in terms of the real parts of \( g_m^{LF} \) and \( g_m^{HF} \), and since, \( C_{it} = qD_{it} \), the interface trap density, \( D_{it} \) can be expressed as:
\[ D_{st} = \frac{I_D C_{ox}}{kT} \left[ \text{Re} \left\{ \frac{1}{g_{\text{m LF}}} \right\} - \text{Re} \left\{ \frac{1}{g_{\text{m HF}}} \right\} \right] \]  

(6.4)

The set-up consists of two voltage sources and a lock-in-amplifier as shown in fig. 6.1. The lock-in-amplifier is preceded by a current to voltage converter with high transconductance gain. The transistors are biased in weak inversion. A time varying sinusoidal excitation tapped from the internal oscillator of the lock-in-amplifier is superposed on the dc bias applied to the gate terminal of the device. The superposition of the signals has been achieved through an operational amplifier in adder configuration as shown in fig. 6.2. Since the ac component of gate signal is of the order of 20 mV, the AC signal fed to the adder is attenuated by a factor of 10 so as to achieve a better resolution.

The current to voltage converter converts the time varying component of drain current into voltage, which is then fed to the lock-in-amplifier input terminal. The lock-in-amplifier locks into the signal having identical frequency to that of the AC signal fed in and rejects the other frequency components. Thus, the time varying component of drain current gets accurately facilitating the determination of dynamic transconductance at the given frequency.

The lock-in-amplifier used in the experiments can only generate signals with frequencies up to 100 kHz. However, with the biasing employed in the experiments performed, only the interface traps near the mid-gap are being probed. These traps stop responding for the gate excitations with frequencies in this range. Hence, the method works with the given range of frequencies.
6.2 Experimental Results

6.2.1 Validation of technique on bulk MOSFETs

The experiments were planned in two phases. The first phase comprised of validation of the proposed technique using charge pumping techniques on bulk MOSFETs.

![Fig 6.3: Pre-stress interface state density in SOI conventional MOSFET & JVD MNSFET by multi freq. \( g_m \) technique](image1)

![Fig 6.4: Pre-stress interface-state density in bulk JVD MNSFET and conventional MOSFET as measured using charge pumping](image2)

Fig.6.3 shows the results obtained by the application of this technique on SOI JVD MNSFETs and conventional MOSFETs. The double plateau curve is obtained, as interface traps are unable to follow the gate signal at high frequencies, thereby decreasing the transconductance as given by eqn.(6.2). Thus, interface state density can be extracted using eqn.(6.3). Though the Re\( \{g_m\} \) at low frequency is more for SOI JVD MNSFETs than conventional MOSFETs, the interface state density turns out to be higher after taking into account the \( I_dC_{ox} \) factor. Fig.6.4 shows the charge pumping results in order to extract pre-stress interface state density in identically processed bulk MOSFETs. A nice correlation between the two methods is obtained.

Since, the multi frequency technique in the present case has been used to characterize the front oxide interface in SOI devices, this correlation can be seen as a validation for the proposed technique. Further, the technique was also validated using hot carrier stress studies on bulk MOSFETs. The bulk MOSFETs were subjected to hot carrier stress and the evolution of \( N_{it} \) with stress bias and time was obtained using charge...
pumping as well as the multi frequency transconductance technique. An excellent match between the two methods was obtained in this case also. The experiment was performed on MOSFETs with silicon oxide as gate dielectric. Figures 6.5 (a) and (b) show the evolution of $N_{it}$ with stress time and bias respectively.

![Fig. 6.5](image)

Fig. 6.5: Interface states with stress (a) time and (b) voltage, after performing hot carrier stress on bulk MOSFETs.

### 6.2.2 Hot Carrier Degradation Studies on JVD SOI MNSFETs

After validating the multi-frequency transconductance technique, hot carrier degradation studies on JVD SOI MNSFETs were performed. The devices under study have been fabricated on SIMOX wafers and have 35 nm Si film thickness and 3.1 nm equivalent gate oxide thickness. Fig. 6.6 summarizes the results obtained. The evolution of $N_{it}$ with stress time and bias, for 100 nm channel length SOI JVD MNSFETs was obtained using the multi-frequency transconductance technique. We see from Fig 6.6 (a) that $\Delta N_{it}$ after 1000s of stress is $7 \times 10^{10}$ cm$^{-2}$. This is obtained by assuming that interface states are uniformly generated in the channel and their distribution with energy is a constant (the mid-gap interface state density has been multiplied by 1 eV). If we take into account the fact that interface state generation is confined to the high field region which is $\sim$5% of the channel, $\Delta N_{it}$ in the damage region works out to be $\sim 1.4 \times 10^{12}$ cm$^{-2}$. This is less than the $\Delta N_{it}$ (approximately $3.0 \times 10^{12}$ cm$^{-2}$) obtained in identical bulk MNSFETs for similar stress conditions and time ($V_g = V_d/2 = 1.5V$ for 1000s) [11].
Under these stress conditions, the SOI device is fully depleted. The electric field in the drain region is lower in the fully depleted device than identically processed partially depleted or bulk device [39]. As a result, less electron-hole pair generation takes place in the fully depleted device. Additionally, damage due to substrate hot carriers is not there in fully depleted SOI MOSFETs leading to lesser damage as compared to that in bulk MOSFETs.

6.3 Conclusions

A multi-frequency transconductance technique has been implemented using a lock-in-amplifier for characterizing interface states in deep sub-micron SOI MOSFETs. The results obtained using the set-up are in excellent agreement with the conventional charge-pumping methods down to sub 100 nm MOSFETs.

Using the multi-frequency transconductance technique, 100 nm channel length SOI MNSFETs, with JVD nitride as the gate dielectric, were evaluated under different hot-carrier stress conditions. Hot carrier degradation is found to be less severe in SOI JVD MNSFETs compared to identical bulk devices due to a lower peak electric field in FD SOI, in addition to absence of substrate initiated hot carrier degradation effects in these devices.
This method can be extended for doing energy profiling of the interface traps. Also, the back interface of SOI devices can be characterized by application of this technique. By varying the magnitudes of AC and DC gate excitations, one can probe other traps besides interface traps near the mid-gap. The multi frequency transconductance technique can be also used to evaluate the lifetimes of various traps by suitably adjusting the gate excitation levels. In the present case, only the high and low frequency regimes of the $\text{Re}\{g_m\}$ have been utilized to extract density of interface states. The measurement of lifetimes of the traps will involve the usage of entire range of frequencies and then the full power of this technique will come to the fore.
Chapter 7

Summary and Future Work

This project focussed primarily on developing a set-up for interface characterization in Silicon-on-Insulator MOSFETs. In the initial stages of the project, basic characterization on SOI MOSFETs was done besides, performing simulations in order to gain a complete understanding of working of these devices. Process simulator, TSUPREM-4, and device simulator, Medici were used for doing simulations. As the project progressed, the focus shifted to characterization of SOI devices. A multi-frequency transconductance technique for interface characterization of SOI devices was developed during the second stage of the project. Some work was also done towards gate-induced-leakage-current (GIDL) studies on SOI MOSFETs. These studies were used to characterize the floating body effects in SOI MOSFETs [39-43].

7.1 Summary of Key Results

Interface characterization is of paramount importance in reliability studies of small geometry MOSFETs with novel gate dielectrics. However, most of the techniques developed for characterizing bulk Si MOSFETs cannot be used for modern SOI devices, which have complex dielectrics and small geometry. This is because there is no substrate contact available in these devices. A multi-frequency transconductance set-up was implemented using a lock-in-amplifier. After initial validation of the technique using charge pumping studies on bulk MOSFETs, the technique was employed for hot carrier induced degradation studies in sub 100 nm JVD SOI MNSFETs. The devices used had silicon film thickness of 35 nm and channel width of 10 µm. Hot carrier degradation is found to be less severe in SOI JVD MNSFETs compared to identical bulk devices due to a lower peak electric field in FD SOI, in addition to absence of substrate initiated hot carrier degradation effects in these devices.
Minimization of off-state leakage currents is an important issue in high-density, very low power, battery powered CMOS technologies. The off state Gate-Induced-Drain-Leakage (GIDL) current, caused by band-to-band tunneling in the gate-drain overlap region, therefore, assumes greater significance. Due to the parasitic bipolar action in the floating body, the GIDL current is found to be substantially enhanced in a short-channel SOI MOSFET as compared with bulk devices. The parasitic bipolar current gain values for conventional and LAC SOI MOSFETs were experimentally evaluated using GIDL current technique. LAC SOI MOSFETs have been shown to give rise to reduced floating body effects as a result of lower electric field in the gate-drain overlap region. The extracted parasitic bipolar gain values are an order of magnitude lower for the LAC SOI MOSFETs as compared to those for the conventional SOI MOSFETs. Thus, channel engineering is an effective way to alleviate the floating body effects in deep sub-micron SOI MOSFETs, where the second order effects like GIDL currents cannot be neglected due to the parasitic bipolar action.

### 7.2 Future Work

Besides the usage in interface characterization in SOI MOSFETs, the multi-frequency transconductance set-up can be used for other devices where conventional interface state extraction techniques such as charge pumping cannot be used due to large leakage currents. This is the case with devices having novel high-k dielectric as gate dielectrics. Since, the silicon-dielectric interface is not good in these devices, they have large leakage currents. Also, back interface characterization in SOI devices can be easily done by this technique. In the interface extraction method, only the high and low frequency regimes of transconductance are used. However, if one adjusts the gate signal AC and DC excitations, it is possible to characterize the traps for their response times. This application will bring out the full potential of this technique. The technique can be also extended for energy profiling of the interface traps.

The GIDL current technique can be used for hot carrier analysis in SOI MOSFETs. Significant changes in off-state gate-induced-leakage current as a result of the channel hot-carrier stress in short channel SOI nMOSFETs are observed. By hot carrier stress, electron hole pairs are produced and parasitic bipolar transistor turns on leading to
enhancement of GIDL currents. GIDL current transients have also been used to investigate oxide charge trapping and detrapping in a hot carrier stressed nMOSFET. This technique is based on the principle that the silicon surface field and thus GIDL currents vary with oxide trapped charge. This can be adapted to SOI devices and by monitoring the temporal evolution of GIDL currents, the oxide charge trapping/detrapping characteristics can be obtained.
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List of Publications


